

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	871	(distributed near2 multiplex\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 13:50
L2	1	I1 with ((read or writ\$3)same clock)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 13:52
L3	11	I1 same ((read or writ\$3)same clock)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:05
L4	188	I1 and ((power or energy) near4 (sav\$4 or conserv\$5 or reduc\$5 or low\$3 or minimi\$6 or optimiz\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:39
L5	1778	(read near3 (power or energy))with (sav\$4 or conserv\$5 or optimi\$5 or minimiz\$4 or reduc\$5 or lower\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:03
L6	18732	((select\$5 or adapt\$5 or condition\$5 or control\$4)near4 output) with (latch or flipflop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:06
L7	53	I5 same (latch or flipflop or FF)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:43
L8	12617	((select\$5 or adapt\$5 or condition\$5 or control\$4)near4 output) near5 (latch or flipflop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:06

L9	0	I5 same I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:56
L10	45	I5 and I8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:22
L11	41214	(modified or control\$4)near3 (latch or flipflop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:31
L12	3836	L11 with clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:23
L13	298	L12 with read	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:24
L14	157	L13 with output	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:24
L15	0	L12 with (read near3 active)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:24
L16	105	L12 and (read near3 active)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:26

L17	28	L16 and (clock adj5 phase)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:25
L18	0	L14 same (output adj open)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:26
L19	0	L14 and (output adj open)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:26
L20	26025	(modified or control\$4 or updated or changed)adj3 (latch or flipflop)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:32
L21	25208	(modified or control\$4 or updated or changed)adj3 (latch )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:32
L22	2074	(modified or updated or changed)adj3 (latch )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:32
L23	2170	(modified or updated or changed or corrected)adj3 (latch )	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:33
L24	1	I23 and (output with (clock with (read near2 active)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:37

L25	1	I23 and (output same (clock with (read near2 active)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:52
L26	3172	((retirement adj (payload adj array))or RPA)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:39
L27	266	I26 and ((power or energy) near4 (sav\$4 or conserv\$5 or reduc\$5 or low\$3 or minimi\$6 or optimiz\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:41
L28	2	I26 and ((power or energy) near3 dissipat\$4) with read)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:41
L29	5	I26 and (read with ((power or energy) near4 (sav\$4 or conserv\$5 or dissipat\$4 or reduc\$5 or low\$3 or minimi\$6 or optimiz\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:44
L30	8522	(read with ((power or energy) near4 (sav\$4 or conserv\$5 or dissipat\$4 or reduc\$5 or low\$3 or minimi\$6 or optimiz\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:44
L31	13	I30 and (output same (clock with (read near2 active)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 15:52
S1	20971	(read\$4 or access\$4)with (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:34

S2	10223	S1 same (memory or storage or array or ram or cache or cell or ram or rom)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 08:58
S3	6272	S2 and ((limit\$4 or control\$4 or restrict\$4 or disable\$4 or ("not" near2 latch\$4))same (new or "same" or unchanged\$4 or identical or different))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 09:37
S4	796	S2 same ((limit\$4 or control\$4 or restrict\$4 or disable\$4 or ("not" near2 latch\$4))same (new or "same" or unchanged\$4 or identical or different))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 09:08
S5	1285	S1 and ((clock near5 (gat\$4 or restrict\$4 or enable\$4 or disable\$4 or control\$4))same (RPA or read))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:45
S6	66	S5 and (glitch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:00
S7	95	S2 same ((clock near5 (gat\$4 or restrict\$4 or enable\$4 or disable\$4 or control\$4))same (RPA or read))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 09:14
S8	347	((select\$5 or adapt\$5 or condition\$5 or control\$4)near4 output)same (clock with (read near4 (active or enable\$4)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 14:04
S9	70	S8 same (glitch or latch\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:03

S10	7	S8 and (glitch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 09:19
S11	6760	S2 and ((limit\$4 or control\$4 or restrict\$4 or disabl\$4 or ("not" near2 latch\$4) or qualif\$5 or gat\$4) same (new or "same" or unchang\$4 or identical or different))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 09:38
S12	1	S5 and (glitch)	EPO; JPO; DERWENT	OR	OFF	2004/12/29 10:52
S13	941	((read\$4 or access\$4)near5 (activat\$4 or enabl\$4 or restrict\$4 or qualif\$5 or gat\$4))with (new near5 (read or data))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:10
S14	8	S13 same (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:32
S15	2577	(superscalar near2 (microprocessor or processor or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:37
S16	4	S15 same ((read\$4 or access\$4)with (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:39
S17	20308	wallace.inv.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:38
S18	0	S17 and (superscalar near2 (microprocessor or processor or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:38

S19	66570	steven.inv.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:38
S20	100	S19 and (superscalar near2 (microprocessor or processor or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:50
S21	3	S20 and((read\$4 or access\$4)with (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:43
S22	4	S20 and((read\$4 or access\$4)same (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:42
S23	6	S20 and((power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:42
S24	105	(superscalar near2 (microprocessor or processor or controller)) and((read\$4 or access\$4)with (power near3 (dissipat\$4 or consum\$5 or conserv\$5 or sav\$4 or reduc\$5)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 13:49
S25	43	S24 and ((clock near5 (gat\$4 or restrict\$4 or enabl\$4 or disabl\$4 or control\$4))same (RPA or read))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:46
S26	0	S24 and ((reduc\$5 or low\$4 or minimiz\$6)near5 (read near2 power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:48

S27	2	S24 and ((reduc\$5 or low\$4 or minimiz\$6)same (read near2 power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:49
S28	1246	((reduc\$5 or low\$4 or minimiz\$6 or optimiz\$5)with (read near2 power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:49
S29	957	((reduc\$5 or low\$4 or minimiz\$6 or optimiz\$5)near6 (read near2 power))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:49
S30	0	S29 and (superscalar near2 (microprocessor or processor or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:50
S31	470	S29 and ( (microprocessor or processor or controller))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:50
S32	0	S31 and (glitch)	EPO; JPO; DERWENT	OR	OFF	2004/12/29 10:52
S33	25	S31 and (glitch)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/29 10:52

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**1 Reducing power in superscalar processor caches using subbanking, multiple line buffers and bit-line segmentation**

*Ghose, K.; Kamble, M.B.;*

Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on , 16-17 Aug. 1999

Pages:70 - 75

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**2 On reducing register pressure and energy in multiple-banked register files**

*Abella, J.; Gonzalez, A.;*

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**3 A power perspective of value speculation for superscalar microprocessors**

*Moreno, R.; Pinuel, L.; del Pino, S.; Tirado, F.;*

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The Ninth International Symposium on High-Performance Computer Architectu  
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**6 Instruction flow-based front-end throttling for power-aware high-  
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**7 Energy-efficient instruction dispatch buffer design for superscalar  
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**8 A technique to determine power-efficient, high-performance supersc  
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*Zyuban, V.V.; Kogge, P.M.;*

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*Lev, L.A.; Charnas, A.; Tremblay, M.; Dalal, A.R.; Frederick, B.A.; Srivatsa, C. Greenhill, D.; Wendell, D.L.; Duy Dinh Pham; Anderson, E.; Hingarh, H.I.; Razzack, I.; Kaku, J.M.; Shin, K.; Levitt, M.E.; Allen, M.; Ferolito, P.A.; Bartolo R.I.; Yu, R.K.; Melanson, R.J.; Shah, S.I.; Nguyen, S.; Mitra, S.S.; Reddy, V.; Ganesan, V.; de Lange, W.J.;*

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**13 Reducing power requirements of instruction scheduling through dynamic allocation of multiple datapath resources**

*Ponomarev, D.; Kucuk, G.; Ghose, K.;*

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**15 Simplifying instruction issue logic in superscalar processors**

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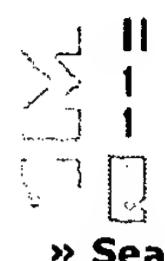
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**1 System-level power consumption modeling and tradeoff analysis techniques for superscalar processor design**

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**2 Energy-efficient instruction dispatch buffer design for superscalar processors**

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Pages:237 - 242

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Conte, T.M.; Menezes, K.N.P.; Sathaye, S.W.;  
System Sciences, 1995. Proceedings of the Twenty-Eighth Hawaii International Conference on , Volume: 1 , 3-6 Jan. 1995  
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**4 Power reduction through work reuse [superscalar processor microarchitecture]**

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*Asato, C.;*  
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**6 Reducing power in superscalar processor caches using subbanking,  
multiple line buffers and bit-line segmentation**

*Ghose, K.; Kamble, M.B.;*  
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Symposium on , 16-17 Aug. 1999  
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**7 A power perspective of value speculation for superscalar  
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*Moreno, R.; Pinuel, L.; del Pino, S.; Tirado, F.;*  
Computer Design, 2000. Proceedings. 2000 International Conference on , 17-2  
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**8 A three-parameter fast Givens QR algorithm for superscalar process**

*Carrig, J.J., Jr.; Meyer, G.G.L.;*  
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**12 Cache designs for energy efficiency**

*Ching-Long Su; Despain, A.M.;*

System Sciences, 1995. Proceedings of the Twenty-Eighth Hawaii International Conference on , Volume: 1 , 3-6 Jan. 1995

Pages:306 - 315 vol.1

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**13 Program balance and its impact on high performance RISC architectures**

*John, L.K.; Reddy, V.; Hulina, P.T.; Coraor, L.D.;*

High-Performance Computer Architecture, 1995. Proceedings. First IEEE Symposium on , 22-25 Jan. 1995

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**14 Conditional annulling for superscalar processors**

*Chun-Hung Wen; Chih-Yuan Cheng; Yun-Yu Kung; Chung-Yu Chang; Yen-Jen Oyang;*

TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering.1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993

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**15 Inherently lower-power high-performance superscalar architecture**

*Zyuban, V.V.; Kogge, P.M.;*

Computers, IEEE Transactions on , Volume: 50 , Issue: 3 , March 2001

Pages:268 - 285

[\[Abstract\]](#) [\[PDF Full-Text \(1616 KB\)\]](#) [IEEE JNL](#)

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 Print Format[Search Results](#) [PDF FULL-TEXT 472 KB] [DOWNLOAD CITATION](#)**A 14-port 3.8-ns 116-word 64-b read-renaming reg file**

Asato, C.

HAL Computer Systems Inc., Campbell, CA, USA;  
*This paper appears in: Solid-State Circuits, IEEE Journal of*

Publication Date: Nov. 1995

On page(s): 1254 - 1258

Volume: 30 , Issue: 11

ISSN: 0018-9200

Reference Cited: 1

CODEN: IJSCBC

Inspec Accession Number: 5173164

**Abstract:**

A 116-word by 64-b register file for a 154 MHz four-issue **superscalar processor** renames **read** addresses and **reads** data in a single operation. A 10-port, 116 comparison unit and a rename logic unit use static-bit-line techniques in the c logic. Pulsed-**power** sense amplifiers achieve a 3.8-ns **read** delay while dissip less **power** than a nonpulsed circuit

**Index Terms:**

CMOS digital integrated circuits microprocessor chips read-only storage 0.4 micron  
3.6 W 3.8 ns 64 bit ROM four-issue superscalar processor pulsed-power sense  
read addresses read-renaming register file rename logic unit static-bit-line technique  
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**1 Deterministic clock gating for microprocessor power reduction**

*Hai Li; Bhunia, S.; Chen, Y.; Vijaykumar, T.N.; Roy, K.;*  
The Ninth International Symposium on High-Performance Computer Architectu 2003. HPCA-9 2003. Proceedings. , 8-12 Feb. 2003  
Pages:113 - 122

[\[Abstract\]](#) [\[PDF Full-Text \(350 KB\)\]](#) **IEEE CNF**

**2 Mixed-clock issue queue design for energy aware, high-performance cores**

*Rapaka, V.S.P.; Talpes, E.; Marculescu, D.;*  
Design Automation Conference, 2004. Proceedings of the ASP-DAC 2004. Asia South Pacific , 27-30 Jan. 2004  
Pages:380 - 383

[\[Abstract\]](#) [\[PDF Full-Text \(541 KB\)\]](#) **IEEE CNF**

**3 A mixed-clock issue queue design for globally asynchronous, locally synchronous processor cores**

*Rapaka, V.S.P.; Marculescu, D.;*  
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